Power On Conditions for the X9258

Introduction

The process of powering up a part like the X9258 can be challenging. There are up to five different supply voltages connected to the part. Because of the protection mechanisms built into the device there is a lot of flexibility in how the supplies power-up. However, not all possible power supply conditions can be handled internally.

The power supply issue is complicated further, because as the various voltages are applied to the part, initial conditions are being recalled from internal registers. These recalled values set the wiper position and initialize of the serial interface circuit.

There are two main failure conditions that result from improper power on sequencing. These are:

1. Damage to the device due to latchup caused by reverse voltage application.
2. Improper Power On Recall (POR) of initial conditions.

This document explores the failure mechanisms and recommends conditions for consistent device operation.

Power Supply Limits

The following conditions are specified in the data sheet and MUST be observed. Failure to follow these recommendations can result in device failure or improper Power On Reset (POR).

1. The V- supply is NOT to go more positive than V_{SS} by more than 0.5V at ANY time.
2. The V+ supply is NOT to go more negative than V_{SS} by more than -0.5V at ANY time.
3. The V_{CC} supply is NOT to go more negative than V_{SS} by more than -0.5V at ANY time.

NOTES: It is advised that the excursions above be limited to <0.3V if possible to minimize leakage effects. If any of the above situations is possible, then it is highly recommended that a clamping diode (schottky required) be added to the circuit to protect the DCP device and any other devices connected to that supply.

V_{CC} Supply Quality

The following conditions are highly recommended for proper POR:

1. The V_{CC} supply should power up with a maximum ramp rate 50V/ms and minimum ramp rate of 0.2V/ms (as per the data sheet). See Figure 2.
2. The voltage ramp on V_{CC} should be monotonic (does not reverse direction) and contain no noise greater than 100mV. See Figure 3.
3. Noise or voltage direction changes are especially significant when V_{CC} is in the range of 1.9 to 2.4V. See Figure 4.
4. If the voltage on V_{CC} reaches 1.9 to 2.4V, but has not reached 2.7V, and then falls to less than 1V, it must recover to 2.4V within 1ms or remain below 1V for more than 10ms. This is a "brownout" condition. A brown-out condition that happens before V_{CC} reaches the 1.9 to 2.4V region or when V_{CC} is greater than 2.7V always retains the proper configuration. See Figure 4.

NOTES: It is possible for devices to function properly while violating one or more of these recommendations. However, these conditions are recommended to provide proper POR over a wide range of environmental, system and fabrication variations.

Power Supply Sequencing

Starting with all V_{CC}, V-, V+ and V_{SS} at 0V. For proper POR, the recommended power on sequence is:

1. V_{SS}.
2. V-. V_L can be connected to V- and power up simultaneously with V-.
3. V_{CC}.
4. V+. V_H can be connected to V+ and power up simultaneously with V+.
5. V_W, V_L and V_H (Potentiometer Voltages) last. V_L and V_H can power up earlier as indicated above.
6. V- should be at least -2.7V as V_{CC} reaches 2V. If not, the POR circuit is more susceptable to V_{CC} noise and V_{CC} power-up brown-out conditions. See Figure 5.
7. V_{CC} and V+ should be greater than 2V within 100ms of V- reaching the maximum value of V-. This condition has not been known to cause POR issues, but it can stress the device as the result of improper biasing. See Figure 6.

NOTES: It may be possible to power up V+, V- and V_{CC} simultaneously, or in other sequences, if V_{CC} Supply Quality conditions are met.

If the power sequencing cannot be guaranteed, then it is important to do the following:

- Add resistors to V_H, V_L and V_W to limit the current to less than 10mA into any of the terminals as shown in Figure 1.
- Make sure that the V_{CC} power supply is a clean, monotonic ramp that meets the specified ramp rate conditions.

Supplemental Information

V- must go to a negative value first because this controls the substrate voltage, which must be stable prior to the V_{CC} turn on. This is because the Power on Recall circuit, which recalls the E2 memory contents, has a V_{CC} trip point of about 2.2 volts when V- is in the range of -2.7 to -5.0 volts. But if V- is at 0 volts then the POR trip point drops from 2.2 volts to about 1.9 volts and the recall operation happens at a voltage that is lower than the design value. Also, an unasserted V- input can be pulled above V_{SS} by the application of the V+ supply in some applications, increasing the chance of incorrect wiper recall.

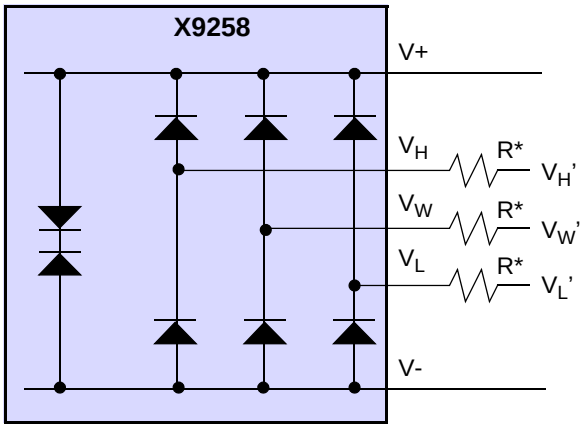
V_{CC} must turn on 2nd with a ramp rate between 0.2V/ms and 50V/ms. This is required because the POR operation must be performed to set the correct wiper position before power is applied to the DCP pins (V_H and V_L). Otherwise the wiper setting could be unknown, allowing possibly excessive currents to flow between the DCP pins and the external circuits. If the ramp rate is too slow, the POR occurs when V_{CC} is too low and the wiper data may be recalled incorrectly. If the ramp rate is too fast, the POR circuit responds before the internal circuits have had a chance to “charge up”, again causing a recall when the voltage internal to the device is too low.

V+ should turn on after V_{CC} powers up because the correct wiper position will have been recalled, leaving no chance of a transient erroneous wiper setting.

V_H, V_L and V_W voltages are generally applied last (with the exceptions noted above). This will assure a uniform power-on at the correct wiper setting and no stress on the internal circuits.

Incorrect Sequencing Issues

The X9258 has protection diodes on each of the supplies as shown in Figure 1.



NOTE: If the power-on sequence cannot be controlled, resistors are required to protect against a worst case condition, where V_H', V_L' or V_W' experience voltage levels that reach V+ or V-. Current should be limited to 10mA, so a 270Ω resistor is required for V+/V- of 2.7V and a 500Ω resistor is required for V+/V- of 5V.

FIGURE 1. X9258 INTERNAL PROTECTION DIODES

V_H, V_L, V_W

If these pins are powered out of sequence, and there are no current limiting resistors, then it is possible to forward bias a PN junction on the chip (which should always be reverse biased). If this occurs, damage to the chip can occur.

V-

If V- powers up more than 100ms before V_{CC} and V+, then internal biasing causes the un-controlled wiper selection FETs to partially turn on. This causes current leakage between V+ and V-.

Improper sequencing can cause these general issues:

8. Permanent damage which appears to be a stuck wiper position that can't be moved or set properly.
9. An SCR latchup condition which can cause large transient currents resulting in permanent damage to the device.
10. Improper recall of the non-volatile wiper setting and in rare cases improper initialization of the serial port.
11. Long term degradation of internal circuits with unknown failure mechanisms.

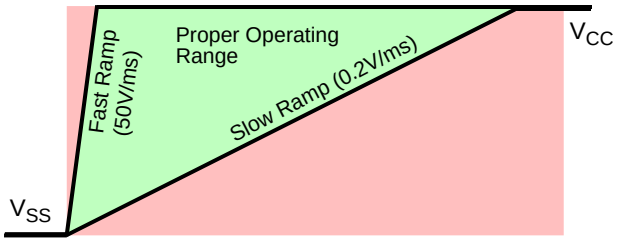


FIGURE 2. V_{CC} RISE TIME

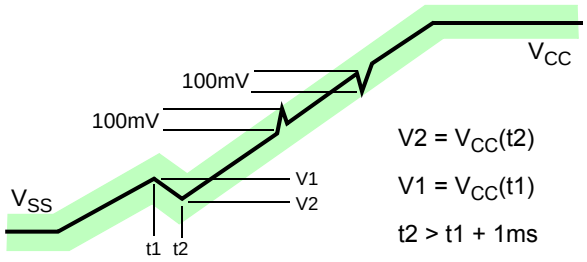


FIGURE 3. V_{CC} MONOTONICITY AND NOISE RESTRICTIONS

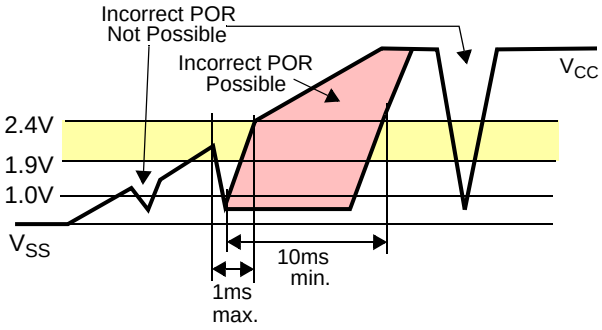


FIGURE 4. V_{CC} POWER-ON BROWN-OUT CONDITION

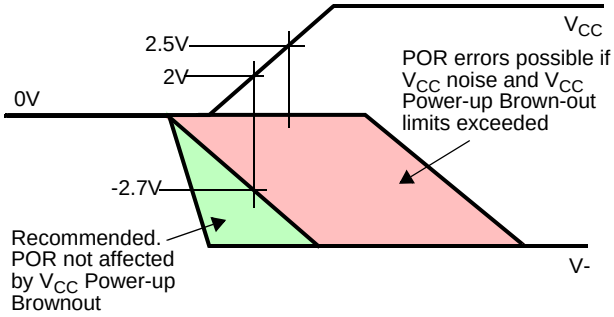


FIGURE 5. V-/V_{CC} POWER-ON TIMING

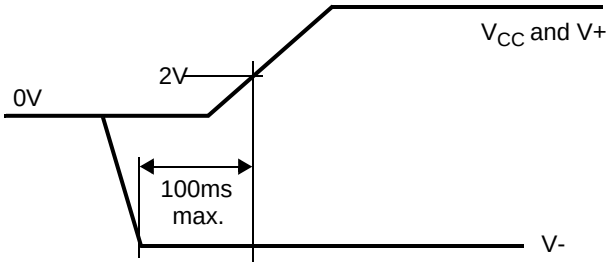


FIGURE 6. V-/V_{CC}/V+ Power-on Timing